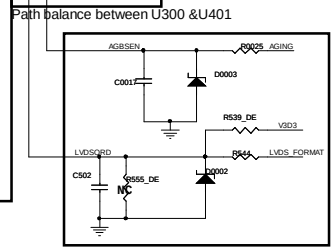


Normal / Mirror Setting Table		
	Normal	Mirror
YDIOU	0	X
YDIOD	X	0
U_DF	H	L
U_DB	L	H

High Aging

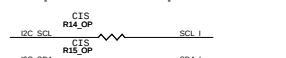
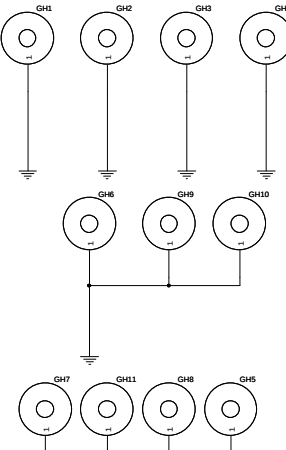
high Aging

Path balance between U300 & U401



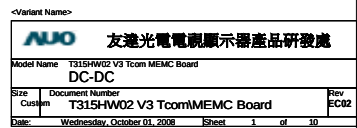
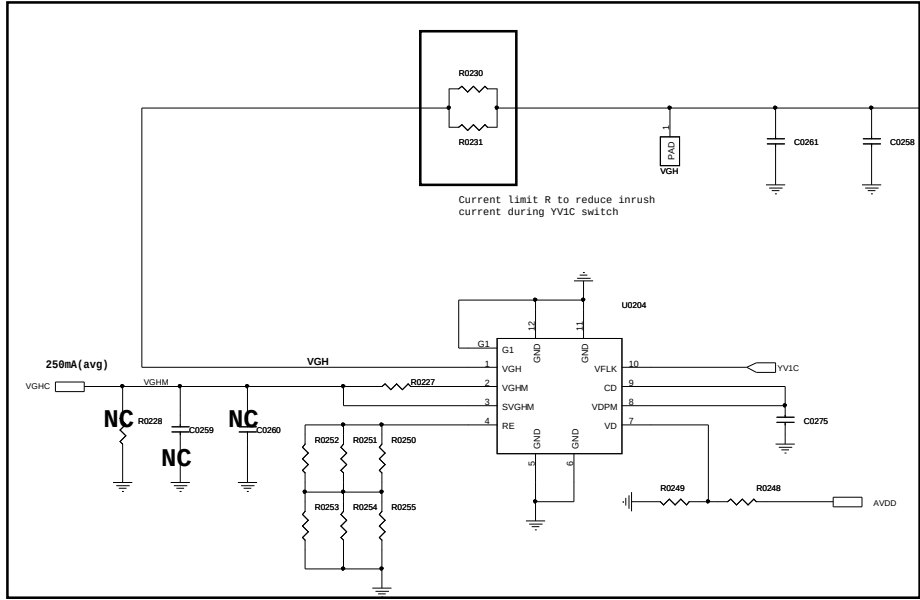
$$T_d(\text{sec}) = R(\Omega) \cdot C(F) \cdot 0.79$$

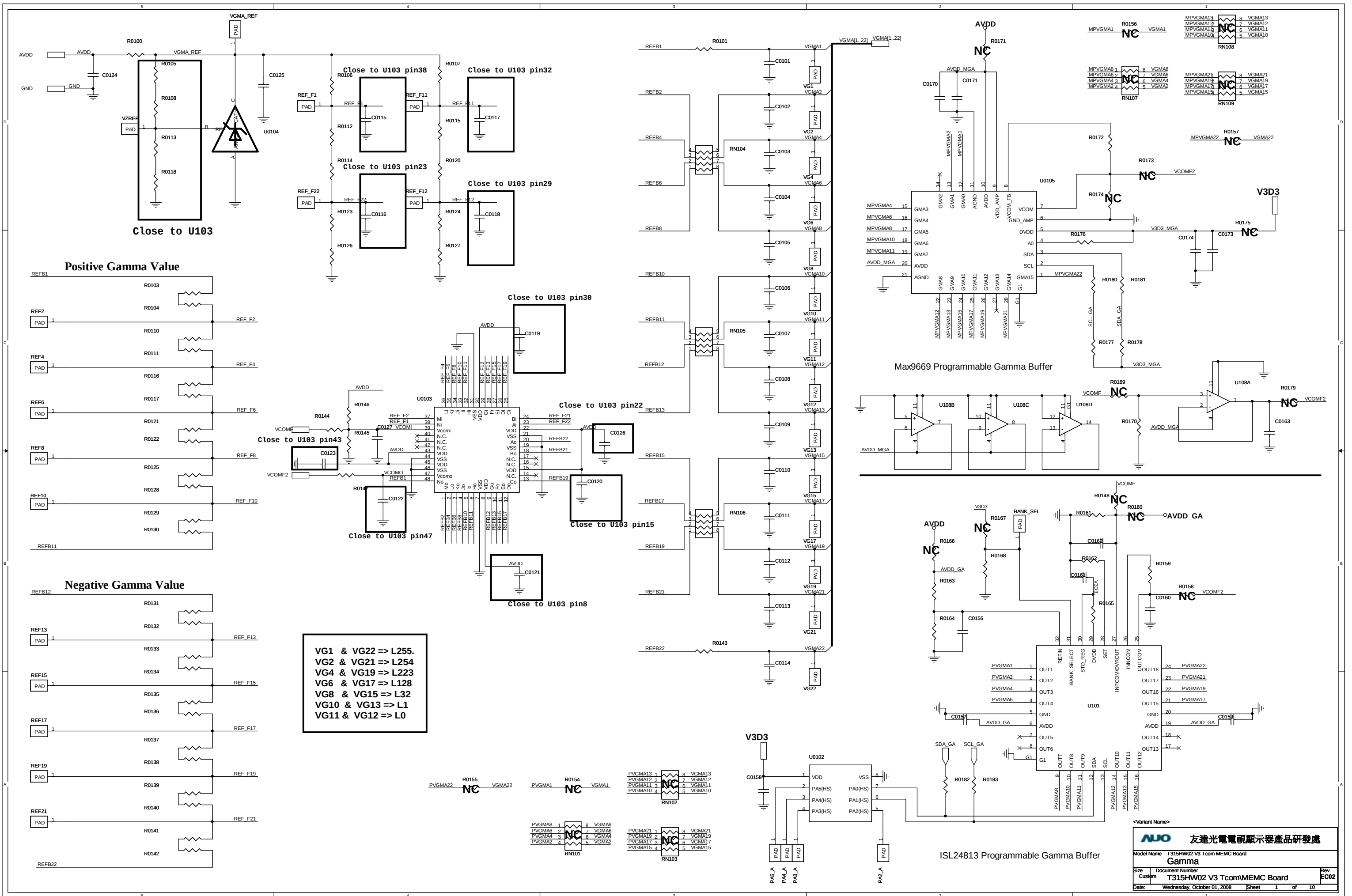
$$= 0.022\mu \cdot 5.62M \cdot 0.79 = 97\text{ms}$$

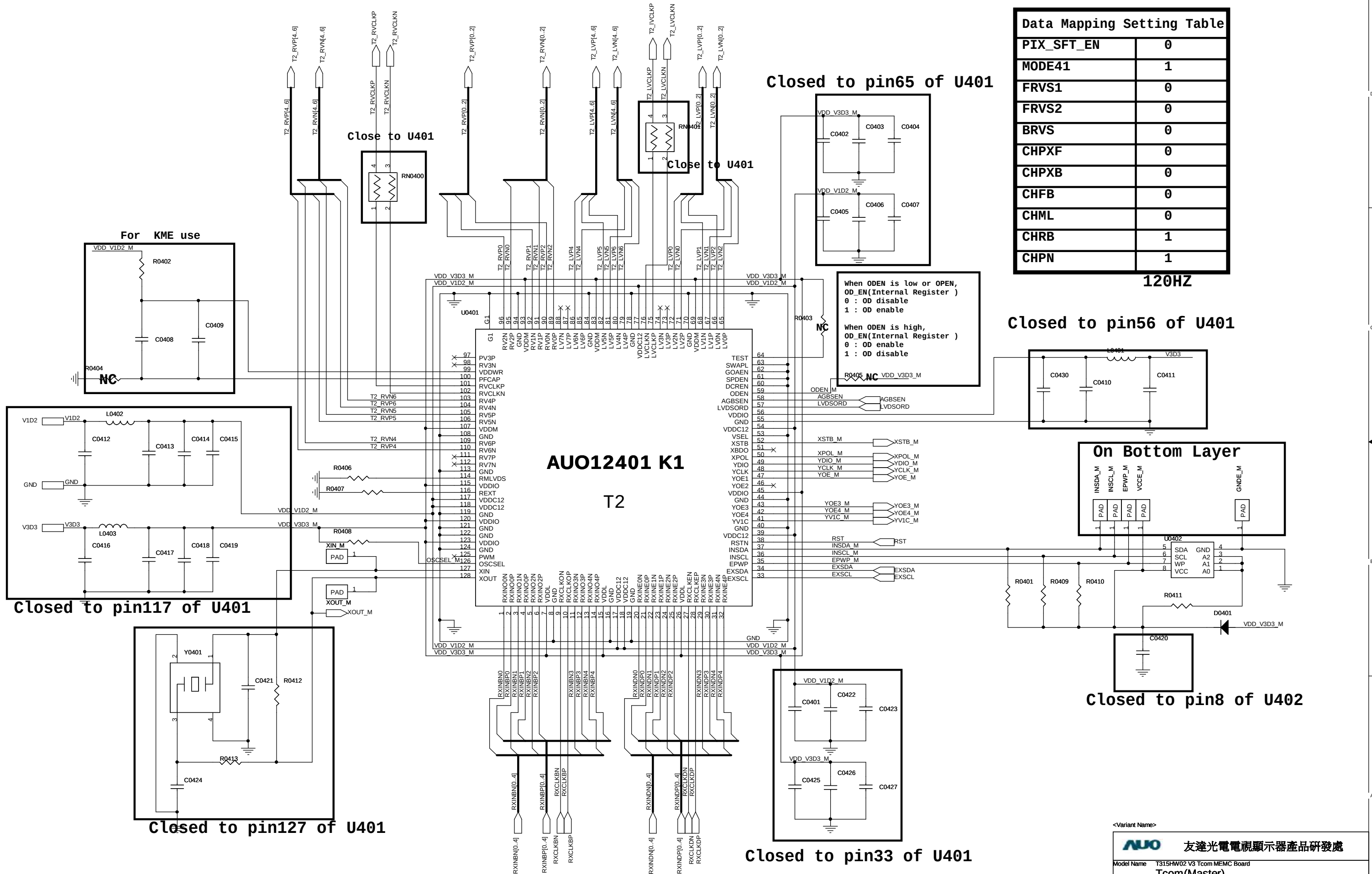


The block diagram illustrates the internal components and connectors of the FRC PART. The components are arranged as follows:

- DC-DC**: A large rectangular block on the left side.
- GAMMA**: A rectangular block on the right side.
- U0300**: A component labeled "T-CON_1(Slave) AU0-12401 B1" with a pin count of "1".
- U0401**: A component labeled "T-CON_2(Master) AU0-12401 B1" with a pin count of "1".
- FRC PART**: A large central block containing:
 - IC500**: A rectangular block.
 - DDR**: Two rectangular blocks, one above and one below IC500.
- Connectors**:
 - CN2615**: A "Power Connector(4Pin)" at the bottom left, with pins 1 and 4 indicated.
 - J1**: An "LVDS Connector(51Pin)" at the bottom right, with pins 1 and 51 indicated.
 - I2C Connector(4Pin)**: A connector on the left edge, with pins 1 and 4 indicated.
 - Top Connectors**: Two connectors at the top, each with pins 80, J4, and 1 indicated.



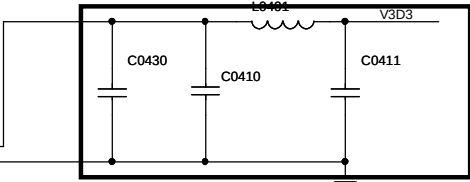




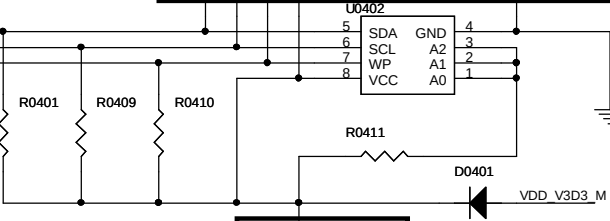
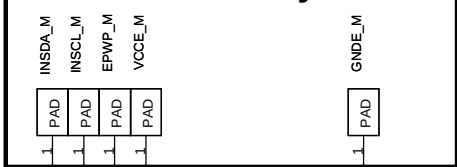
PIX_SFT_EN	0
MODE41	1
FRVS1	0
FRVS2	0
BRVS	0
CHPXF	0
CHPXB	0
CHFB	0
CHML	0
CHRB	1
CHPN	1

120HZ

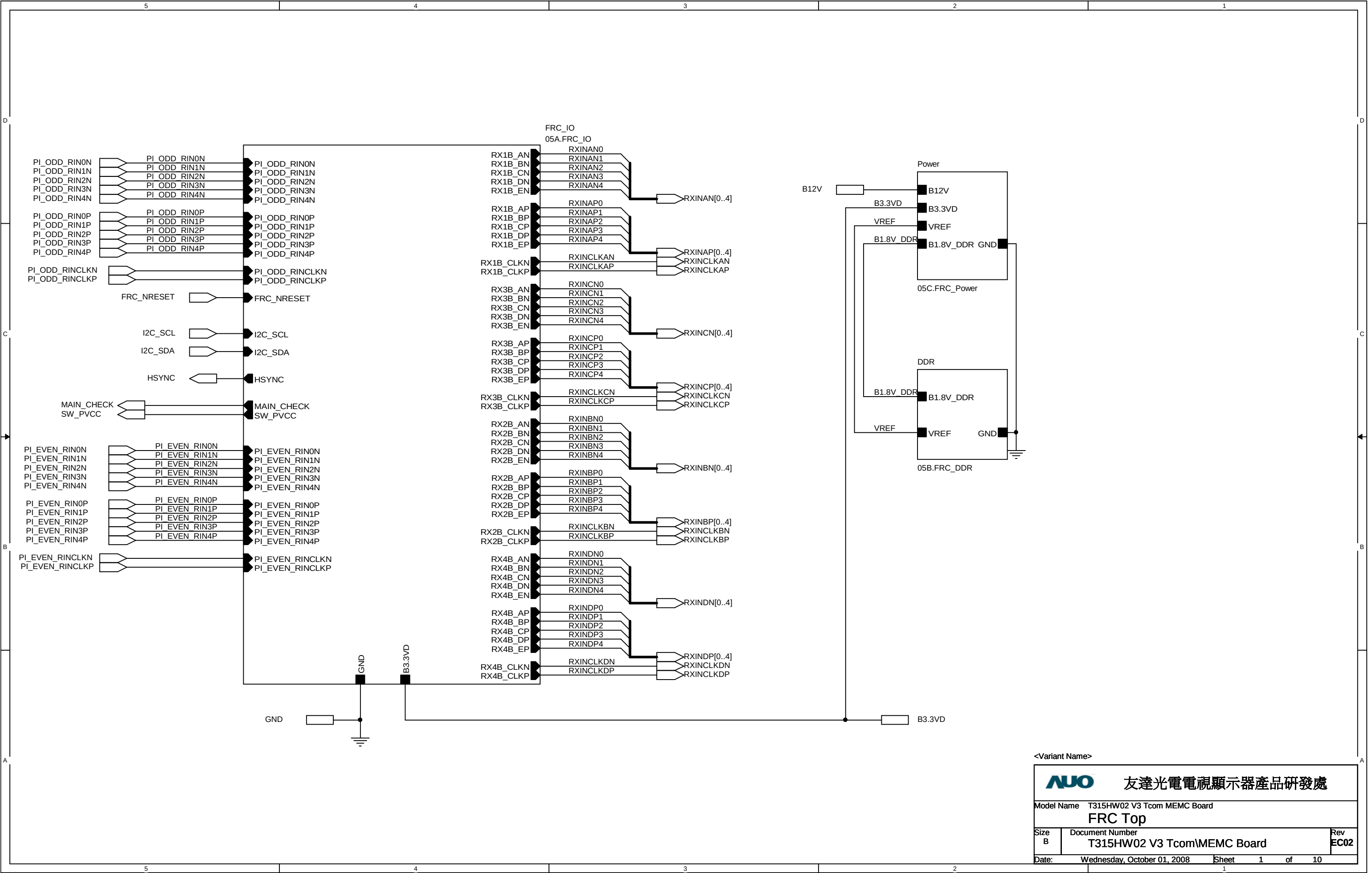
Closed to pin56 of U401

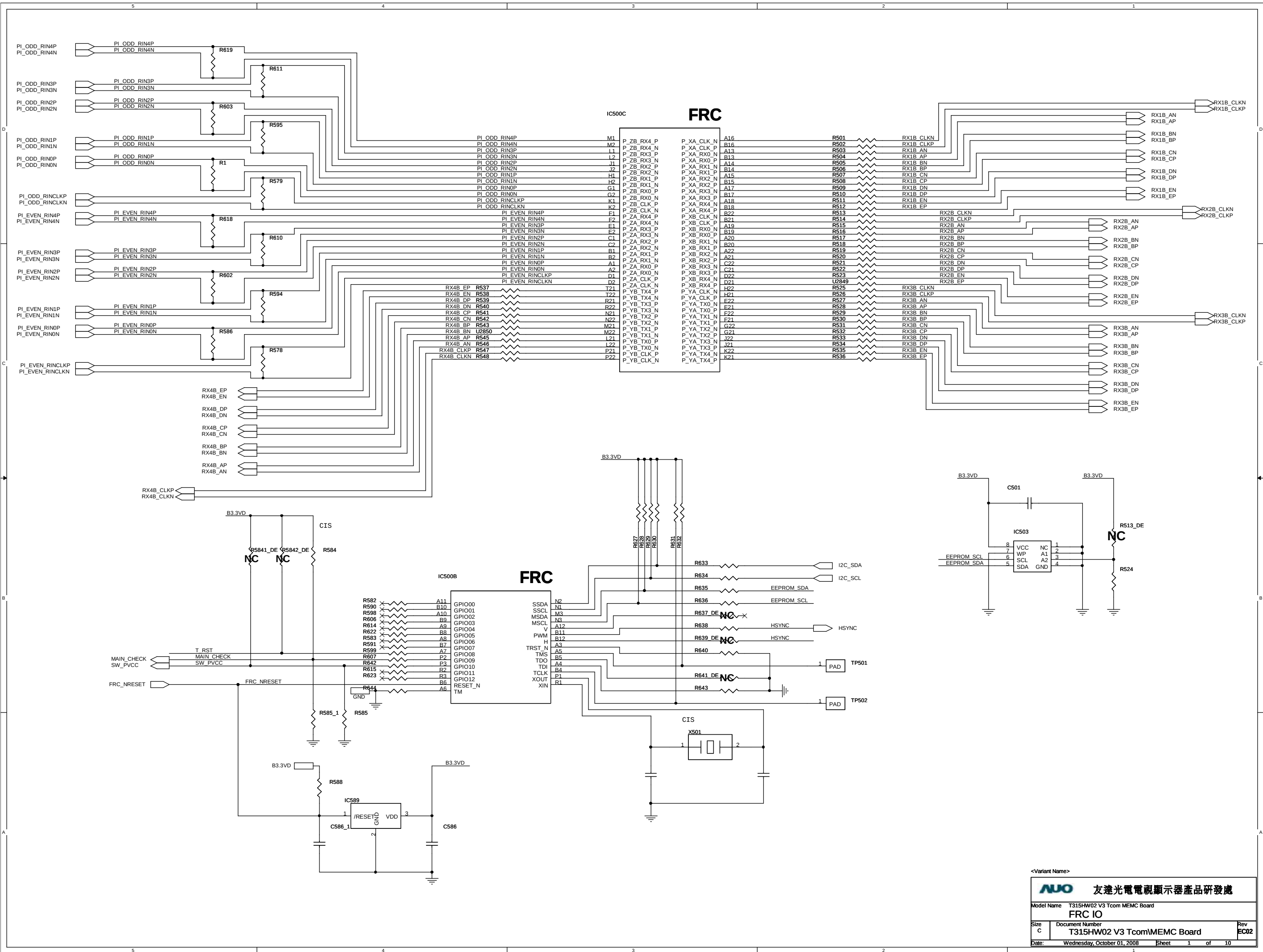


On Bottom Layer



Closed to pin8 of U402





<Variant Name>

友達光電電視顯示器產品研發處

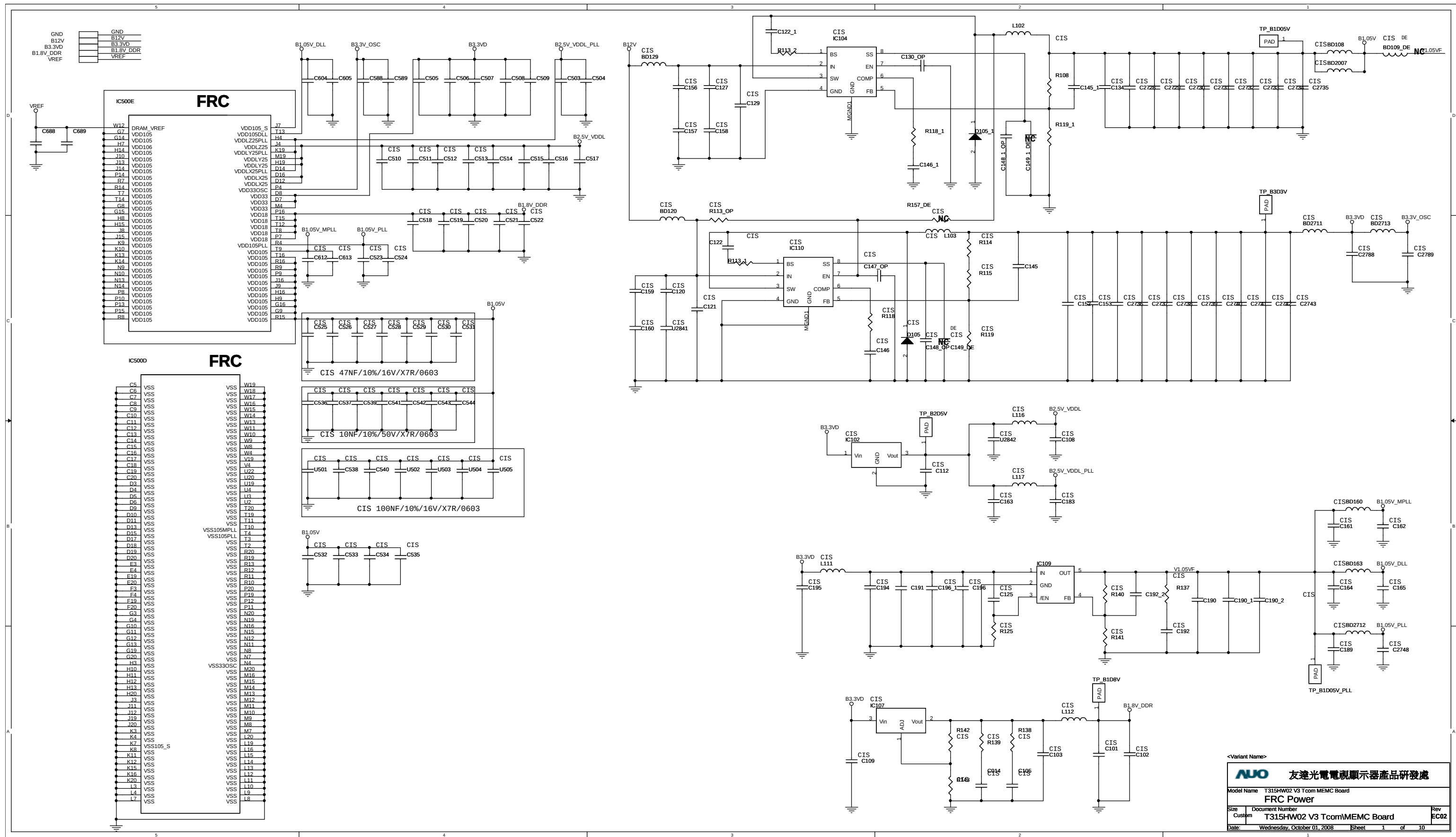
Model Name T315HW02 V3 Tcom MEMC Board

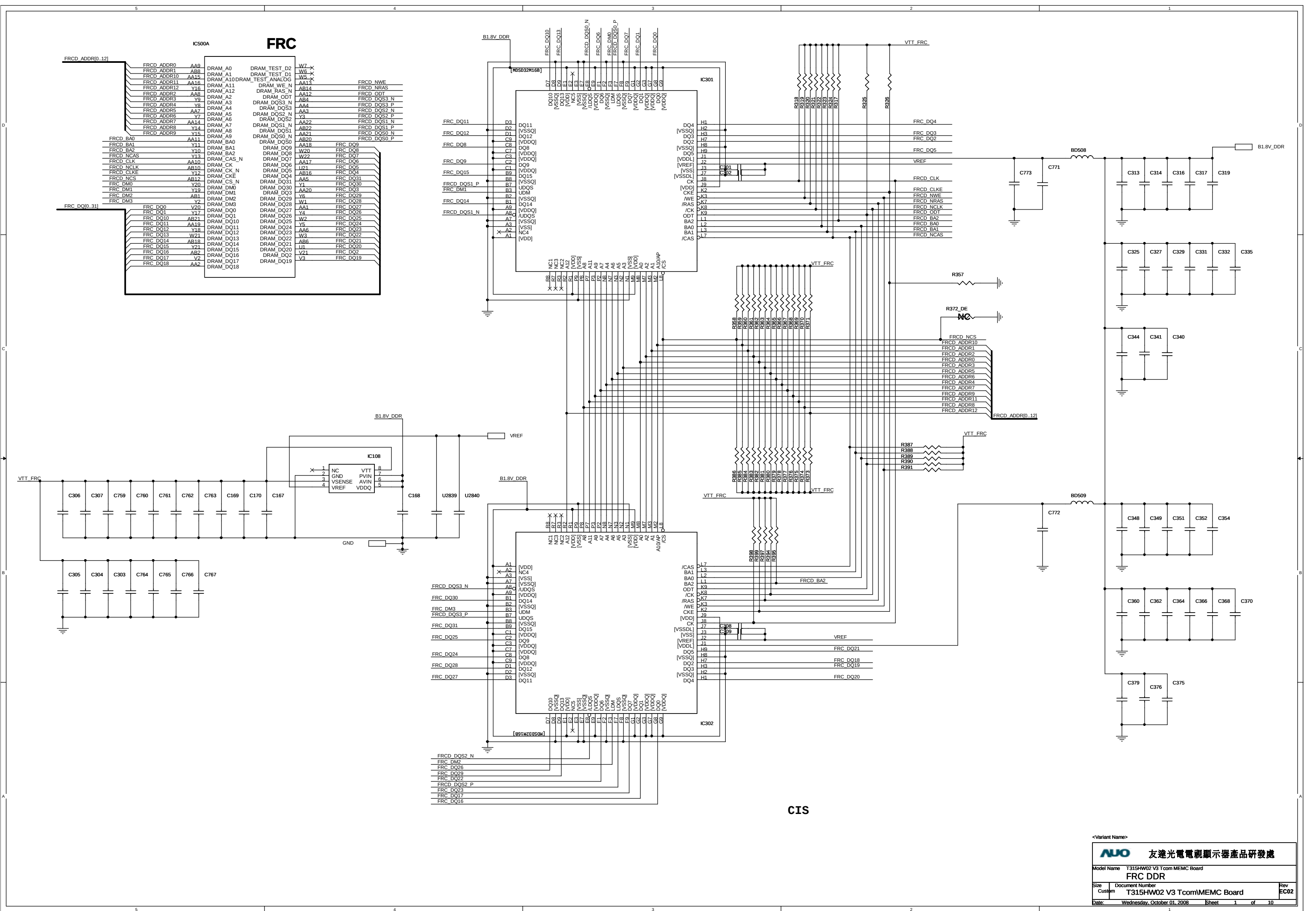
FRC IO

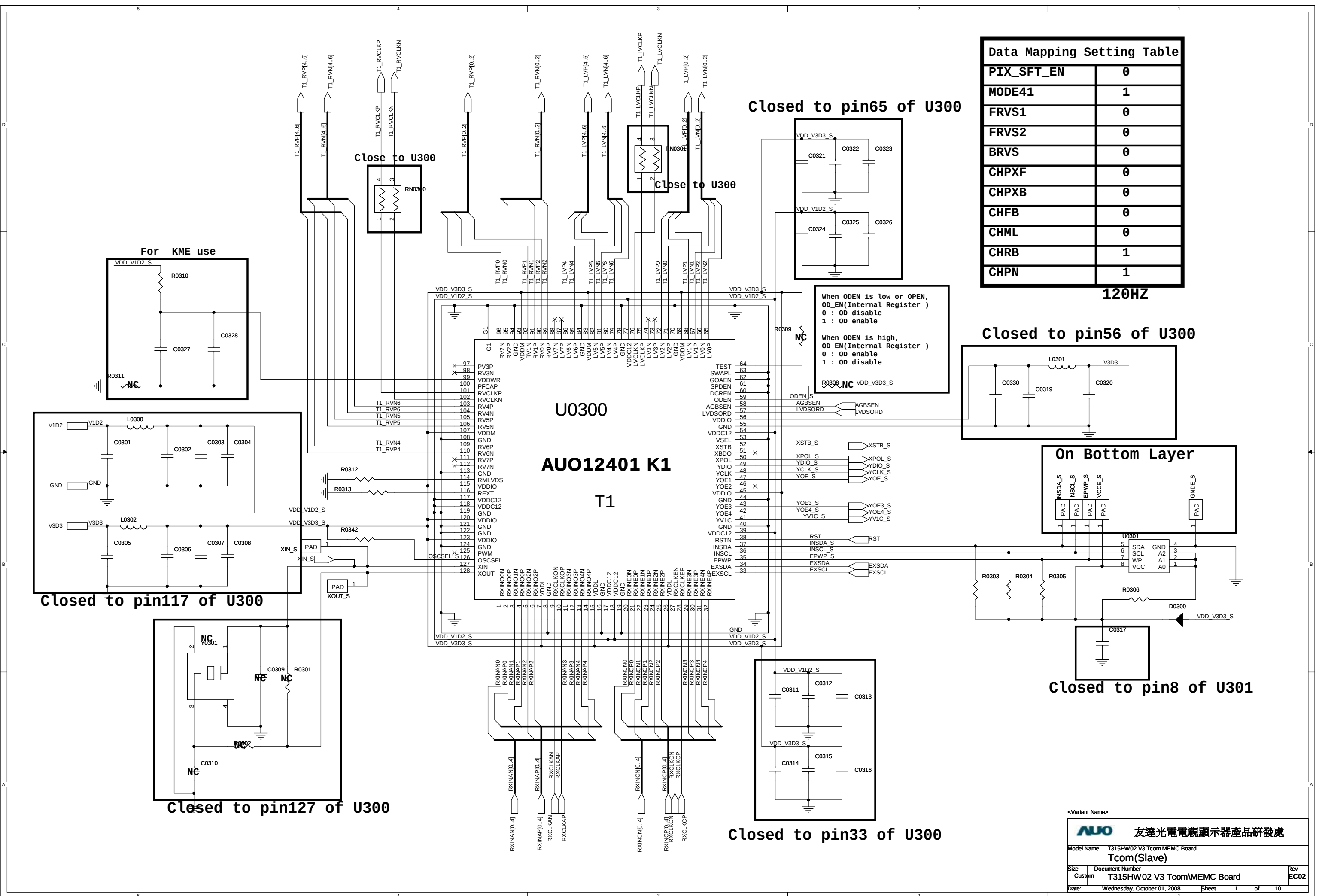
Size C Document Number T315HW02 V3 Tcom\MEMC Board

Date: Wednesday, October 01, 2008 Sheet 1 of 10

Rev EC02







Data Mapping Setting Table	
PIX_SFT_EN	0
MODE41	1
FRVS1	0
FRVS2	0
BRVS	0
CHPXF	0
CHPXB	0
CHFB	0
CHML	0
CHRB	1
CHPN	1

120HZ

Closed to pin56 of U300

On Bottom Layer

Closed to pin8 of U301

Closed to pin33 of U300